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THESIS

MEASURED NOISE PERFORMANCE OF

A NEW METHOD OF FREQUENCY HOPPING

by

Peter Stanley Buczynski

December 1984

Thesis Advisor: G.A. Myers

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probability of error of 0.001 at 1.6dB SNR was obtained.

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Measured Noise Performance of a New Method of Frequency Hopping

by

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B.S., University of Connecticut, 1979

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requirements for the degree of

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ABSTRACT

A frequency hopping (FH) technique in which symbols are transmitted as unique multiple hop sequences is the basis of this research. The receiver, of primary interest, uses a phase locked loop as a frequency to voltage converter and then uses difference amplifier circuits to compare the received sequence with all utilized sequences for data recovery. This report presents the design and results of this FH technique. A bit probability of error of 0.001 at 1.6 dB SNR was obtained.

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TABLE OF SYMBOLS AND ABBREVIATIONS

b	bandwidth of transmitted signal
d1,d2	transmitted data bits
d1',d2'	recovered data bits
m	data bits per symbol
AVM	analog voltage multiplier
BPF	bandpass filter
BW	total available bandwidth
DAC	digital to analog converter
FH	frequency hopping
FSR	feedback shift register
H	number of hops per sequence
HSG	hop sequence generator
MC	master clock
MUX	multiplexer
N	noise power
PLL	phase locked loop
P/S	parallel to serial converter
S	signal power
SJR	signal to jamming ratio
SNR	signal to noise ratio

T	dwell time per hop
TTL	Transistor-Transistor Logic
VCO	voltage controlled oscillator
VH	voltage hopping

I. INTRODUCTION

With an increasing demand for reliable military communications, frequency hopping (FH) is becoming an important digital communication technique. Documented advantages of FH include a moderate amount of immunity to jamming and multipath interference rejection.

A FH technique using multiple hop sequences to represent a symbol is the subject of this research. In contrast to conventional FH where one bit is transmitted per frequency hop, a system is designed, built, and tested in which symbols are transmitted as unique multiple hop sequences. The receiver uses a phase locked loop as a frequency to voltage converter and then difference amplifier circuits to compare the received sequence with all utilized sequences for data recovery. Performance of this system compares favorably with conventional FH (similar to conventional FSK). A bit probability of error of 0.001 at 1.6 dB SNR is obtained as compared to 10 dB SNR for conventional FH.

This report incorporates the design of the experimental system with the results of performance tests. Chapter II presents a brief comparison of conventional and multiple hop sequence FH techniques along with a general description of the research. A description of the experimental system and it's operation is given in Chapter III. Chapter IV includes the procedure for testing the system and an evalution of performance. Finally, Chapter V presents the conclusions and recommendations of this research.

II. DESCRIPTION OF RESEARCH

A. CONVENTIONAL FREQUENCY HOPPING

Frequency hopping (FH) is a spread spectrum communication technique. The carrier frequency in a FH transmitter "hops" from frequency to frequency according to a predetermined pattern.

Figure 2.1 shows the frequency-time diagram for a conventional FH scheme. Typical FH uses one bit per hop with a frequency offset to distinguish either a "1" (shaded frequency band) or a "0" (cross-hatched frequency band). BW is the total available bandwidth for hopping, T is the dwell time per hop, and b is the bandwidth per hop or bandwidth of the transmitted signal. The bandwidth of the transmitted signal, b, is approximately equal to 2/T.

B. MULTIPLE HOP SEQUENCE REPRESENTATION

The multiple hop sequence scheme differs from conventional frequency hopping in that one symbol is transmitted by sending a unique FH sequence. A symbol represents m data bits thereby requiring 2^m sequences. For example, if m = 3, then 3 data bits are simultaneously transmitted and 8 different sequences are required. Each sequence is composed of H hops. H is arbitrarily selected and not related to m. A frequency-time diagram for a multiple hop sequence scheme (H = 7) is shown in Figure 2.2.

There are two distinct advantages in using multiple hop sequence FH over conventional FH. First, when an integration process is incorporated in the receiver (as is done in this system), the integration is performed over the symbol length or m bits (in contrast to one bit as in conventional

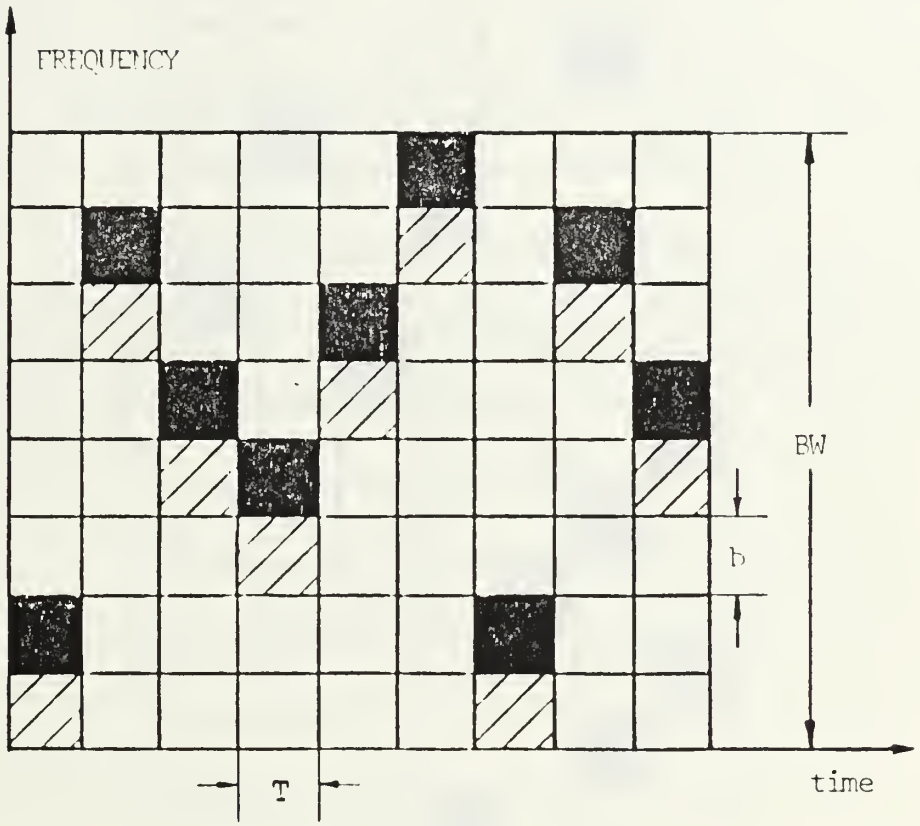

Figure 2.1 Conventional Frequency Hopping

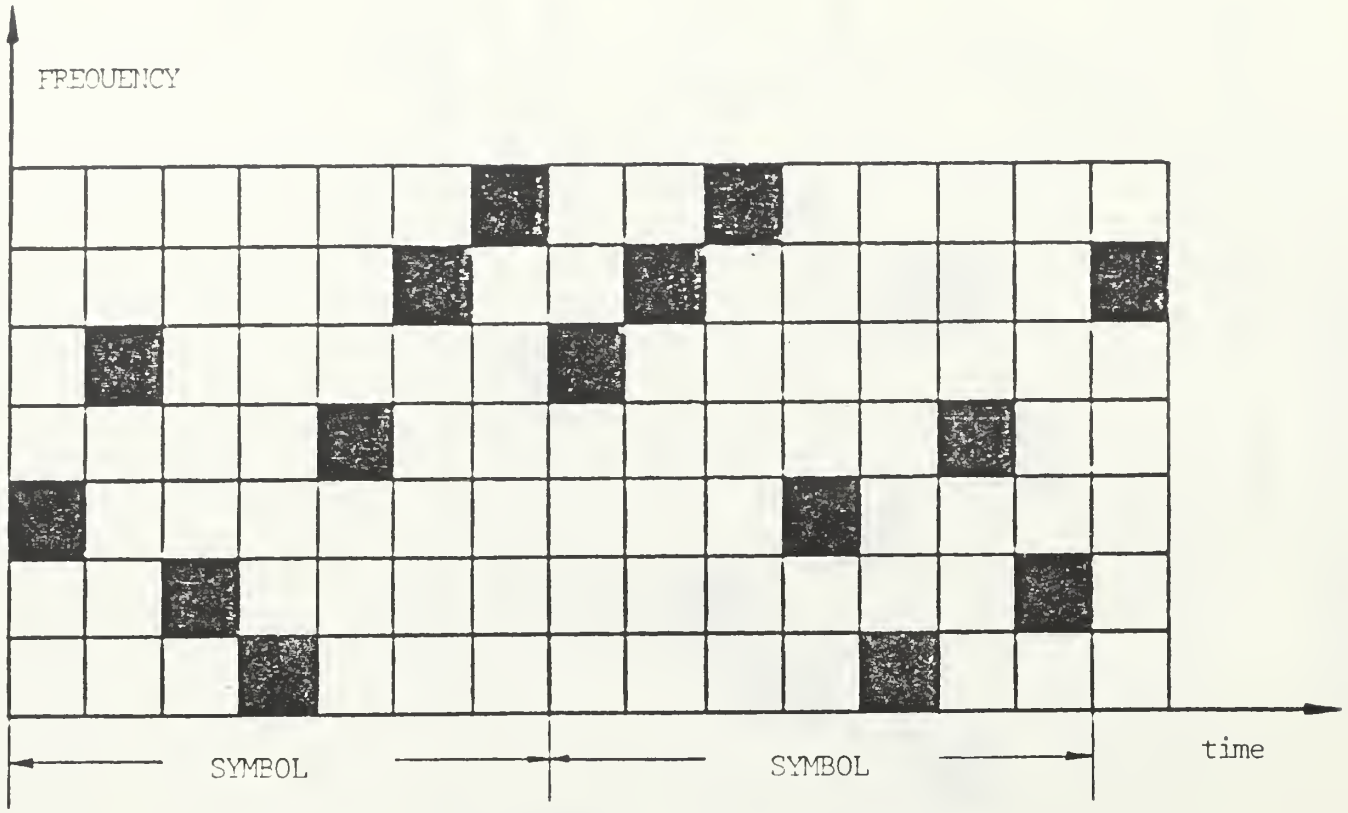

Figure 2.2 Multiple Hop Sequence Scheme

FH). A greater noise reduction is obtained with a longer integration time. Second, greater flexibility in symbol representation is realized when using multiple hop sequence FH. The number of data bits (m) per symbol represented by a particular sequence may be varied. Perhaps more significant is the ability to vary the number of hops (H) per sequence independent of m.

The disadvantage of multiple hop sequence FH is added hardware (complexity). When using a greater number of sequences for data representation, more equipment in the transmitter and receiver is needed. Also, the receiver bandwidth is now BW instead of 2b and so the system noise power is increased by a factor of BW/2b which degrades the system signal to noise ratio. This degradation is partially overcome by the increased integration time available in the receiver.

III. EXPERIMENTAL SYSTEM

A. GENERAL SYSTEM CONSTRUCTION

The experimental system was constructed using standard monolithic integrated circuits and typical electronic circuit components. The integrated circuits and accompanying components were mounted on breadboards. A picture of the experimental system and test equipment is shown in Figure 3.1.

In the transmitter, 2^m different FH sequences are generated. A particular group of m data bits (symbol) selects a particular one of these sequences which is then transmitted. For simplicity, m = 2 and H = 7 thereby requiring the generation of four sequences.

The receiver recognizes the particular FH sequence and recovers the m data bits. Recognition is done by comparing the received sequence with all possible sequences. The manner in which this comparison is made is the main feature of this research.

The problem of synchronization is not addressed in this study. Therefore, the transmitter and receiver use the same clock.

B. SYSTEM COMPONENTS

1. Transmitter

The transmitter is similar to a frequency hopping (FH) transmitter designed by Day [Ref. 1] in which four voltage hopping (VH) sequences are produced by four separate hop sequence generators (HSG). An analog multiplexer selects one of the VH sequences which, in turn, represents a specific data word. The selected VH sequence then produces

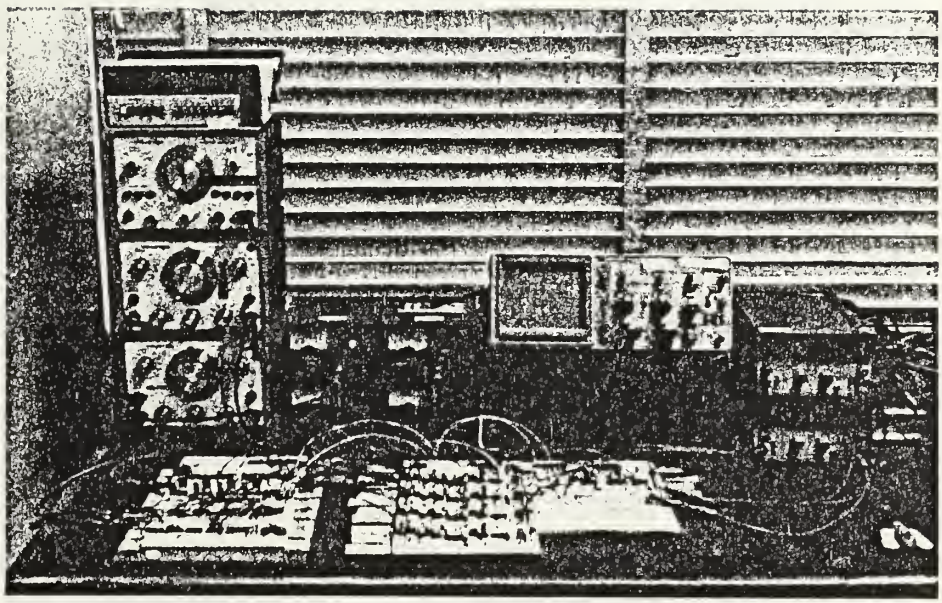

Figure 3.1 Experimental System

the actual FH signal using a voltage controlled oscillator (VCO). A block diagram of the transmitter is presented in Figure 3.2.

The VH sequences are produced by hop sequence generators using maximal length sequences (m-sequences). The hop sequence generators are each composed of a three-stage feedback shift register (FSR) and a digital to analog converter (DAC). Each FSR generates, serially, a seven bit m-sequence and, as a parallel output, seven 3-bit pseudo random words. An Exclusive-Or gate is used for the feedback logic [Ref. 2]. The 3-bit pseudo random words are applied to the DAC which produces a periodic seven-level VH sequence. Figure 3.3 shows one of the four VH sequences.

Each of the four VH sequences (each seven hops in length) represents a two-bit data word or symbol as shown in Table I. In order to obtain four VH sequences, four m-sequences must be generated. Since only two unique m-sequences can be generated from a three stage FSR, VH sequences A and C are delayed and used as VH sequences B and D, respectively.

The delay and start of each VH sequence is chosen to minimize any correlation between the VH sequences. Table I shows the VH sequences represented by the decimal equivalent of the seven 3-bit pseudo random words associated with each m-sequences. To insure that each data word is represented by it's proper VH sequence, all FSR's are reset at the beginning of transmitter operation or when a FSR operates improperly (jumps to a disallowed state, skips a clock cycle, etc.,).

The data words, also generated by a FSR and accompanying circuitry, select the appropriate VH sequence by the use of an analog multiplexer (MUX). The data words are generated by a FSR identical to that used in each HSG except that the FSR has seven stages. This seven stage FSR produces a 127 bit m-sequence composed of 64 "1's" and 63

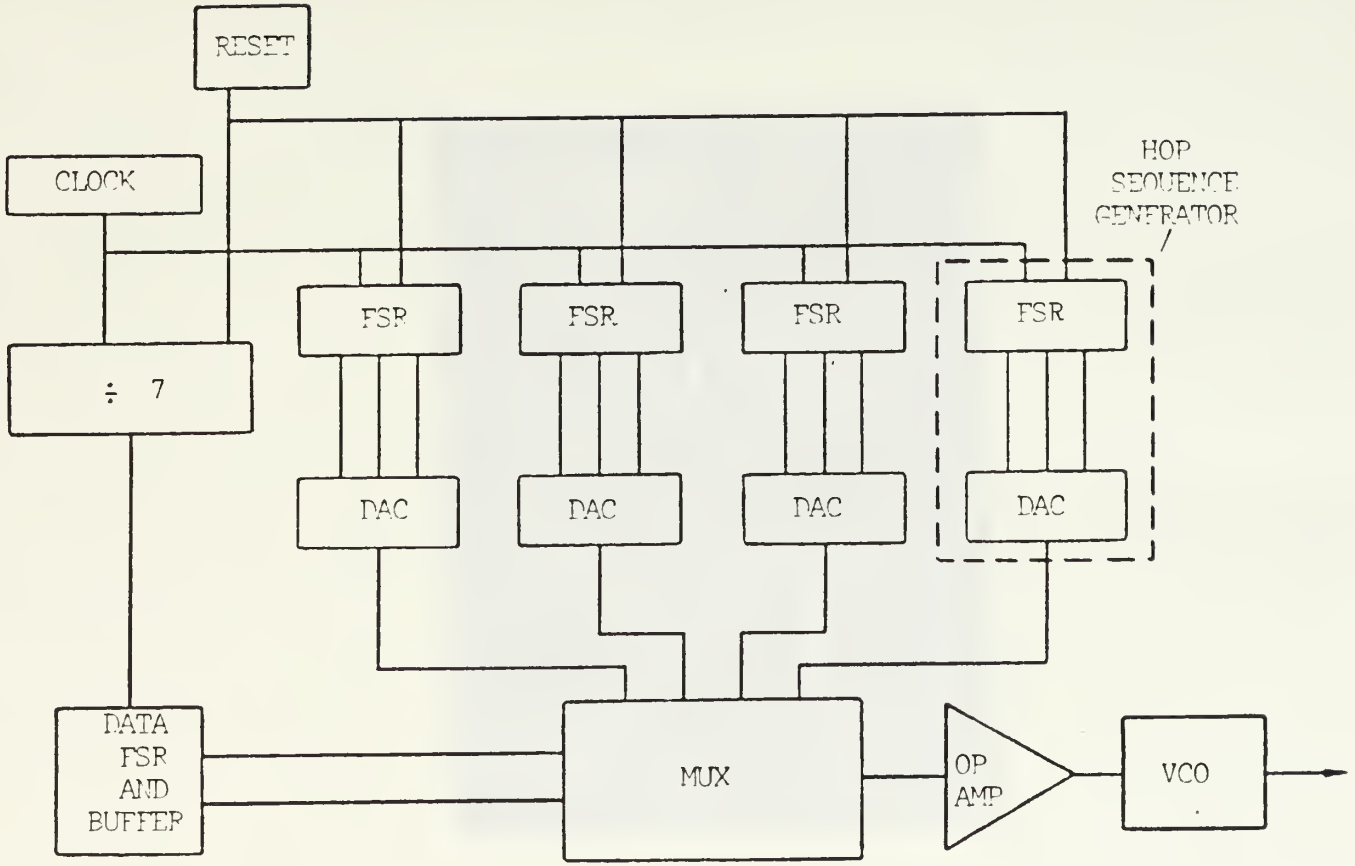

Figure 3.2 Transmitter

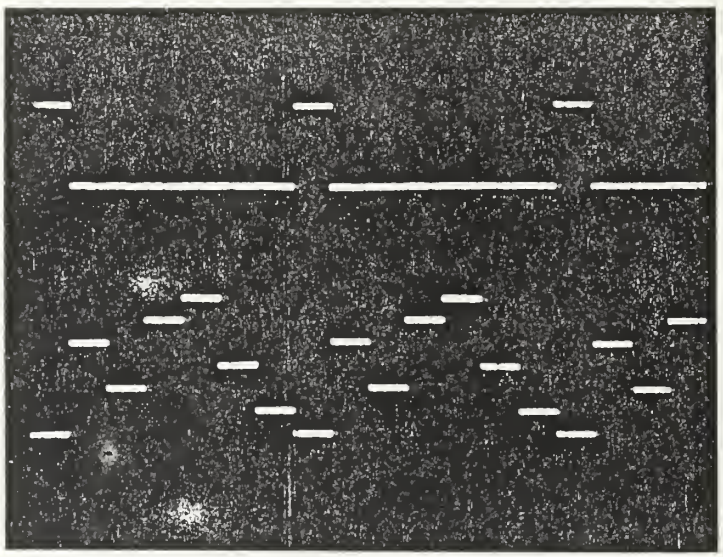

Figure 3.3
Top: Symbol Clock
Bottom: Voltage Hop Sequence, Symbol A

TABLE I

Symbol Sequence

DATA WORD SYMBOL	00 A	01 B	10 C	11 D
SEQUENCE	3	6	5	4
	5	7	6	2
	2	3	7	5
	1	5	3	6
	4	2	1	7
	6	1	4	3
	7	4	2	1

"0's"--adequately "random" to test this system. The two bits making up each data word are tapped from the fifth and sixth stages of the FSR. These two data bits are then buffered, using D-type flip-flops, for proper timing before being applied to the address (or selection) inputs of the MUX. Proper timing is achieved using a clock with a period equal to the length of a VH sequence or, in other words, a clock with a frequency one-seventh that of the clock used for the hop sequence generator FSR's.

The output of each DAC is connected to a channel of the MUX. The proper VH sequence is selected by the data word that appears at the address inputs of the MUX. The selected VH sequence is sent to an operational amplifier (op-amp) circuit and, then, the VCO. The VCO produces the transmitted signal--a FH sinusoid. The op-amp circuit and VCO are adjusted for the desired center frequency, frequency range, and amplitude of the transmitted signal. A detailed circuit schematic of the transmitter is presented in Appendix A.

2. Channel

The block diagram of the circuit used to simulate the channel is shown in Figure 3.4. Somewhat analogous to an actual channel, the transmitted signal is combined with noise within the channel and is then delivered to the front end of the receiver. In the experimental system, Gaussian noise is added to the transmitted signal. The front end of the receiver consists of a bandpass filter (BPF) with a pass band equivalent to the bandwidth of the transmitted signal. This filter represents the IF amplifier/filter of a superheterodyne receiver. The BPF is configured to pass the signal with negligible distortion. A detailed circuit schematic of the channel is presented in Appendix B.

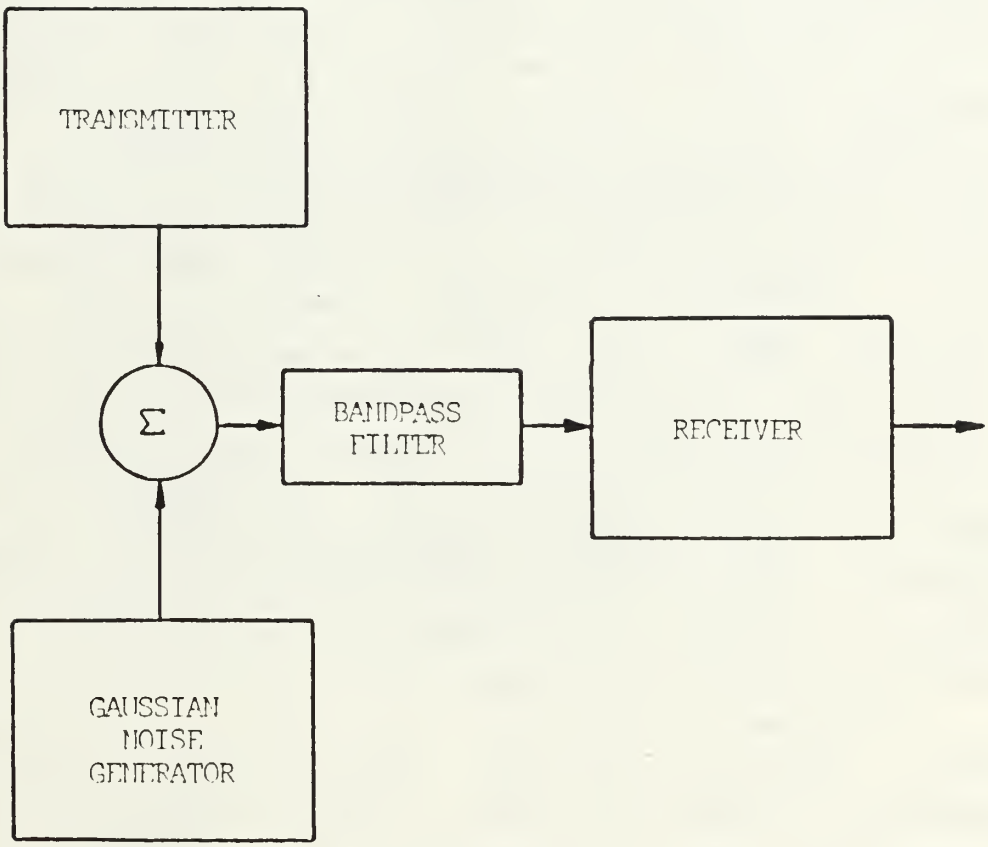

Figure 3.4 System Channel

3. Receiver

The receiver is designed to distinguish the FH sequences and recover the data bits. The received FH signal is converted to a voltage hopping (VH) sequence by a phase locked loop (PLL). This VH sequence is compared to each of the 2^m possible sequences stored in the receiver. The comparison consists of generating the difference of the received and reference sequences in the form of a voltage. If the reference VH sequence is like the received VH sequence, the difference voltage is zero. If the VH sequences applied to a comparison circuit are not alike, then a bipolar multi-level discrete voltage appears at the output of the comparison circuit (Figure 3.5). This is true for all 2^m comparison circuits. Using an analog voltage multiplier (AVM), this output is made unipolar by squaring (Figure 3.5). The squaring process minimizes small voltage differences (low-level noise effects) and augments large voltage differences resulting from the comparison of unlike sequences. The squared difference voltage is integrated (processing gain) and sampled at the end of each symbol interval. A "least of" detector (combinational logic) generates the m bit data word.

The basic components of the receiver are the demodulator, comparison circuits, analog voltage multipliers, integrate and dump circuits, sample and hold circuits, combinational logic, and parallel to serial converter. A block diagram of the receiver is shown in Figure 3.6. Since the problem of synchronization is not addressed in this experimental system, the transmitter and receiver use the same master clock.

To demodulate the received FH sinusoid, a general purpose phase locked loop (PLL) is used (National Semiconductor LM565). The PLL output (or received VH sequence) is shown in Figure 3.7.

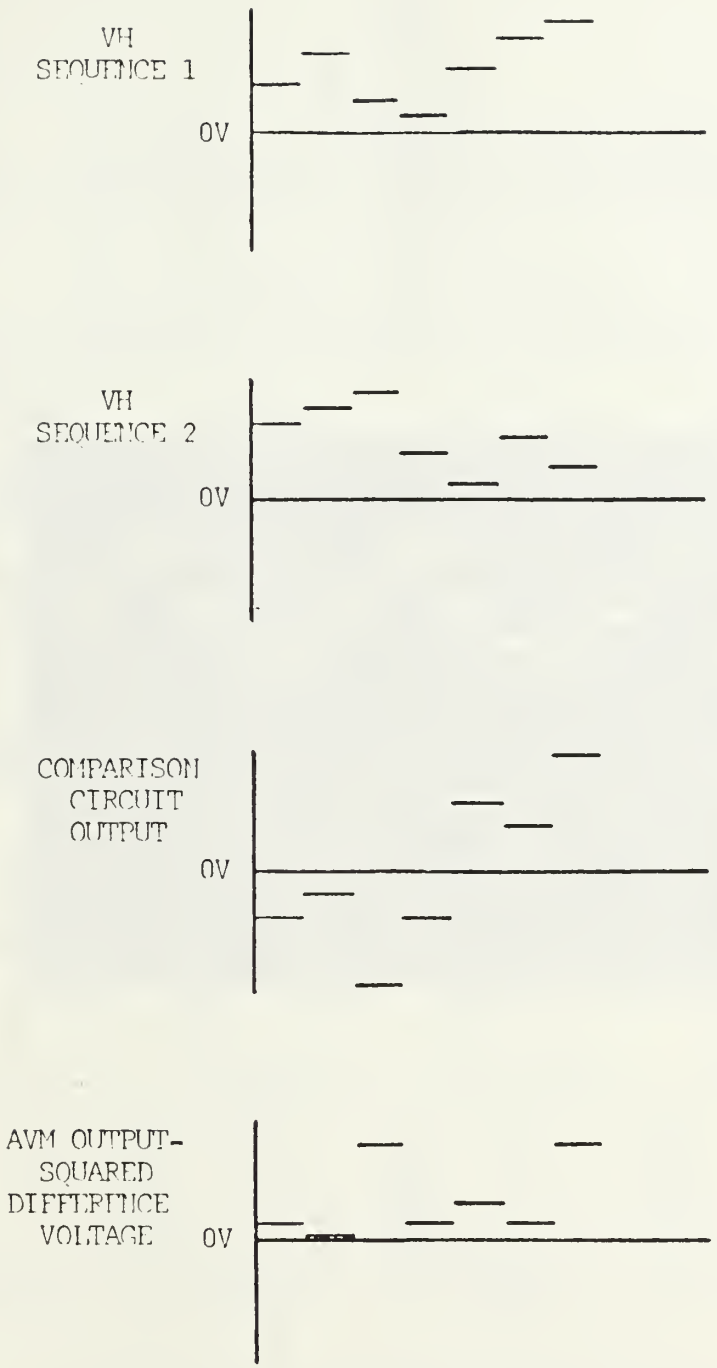

Figure 3.5 Difference Voltage Generation

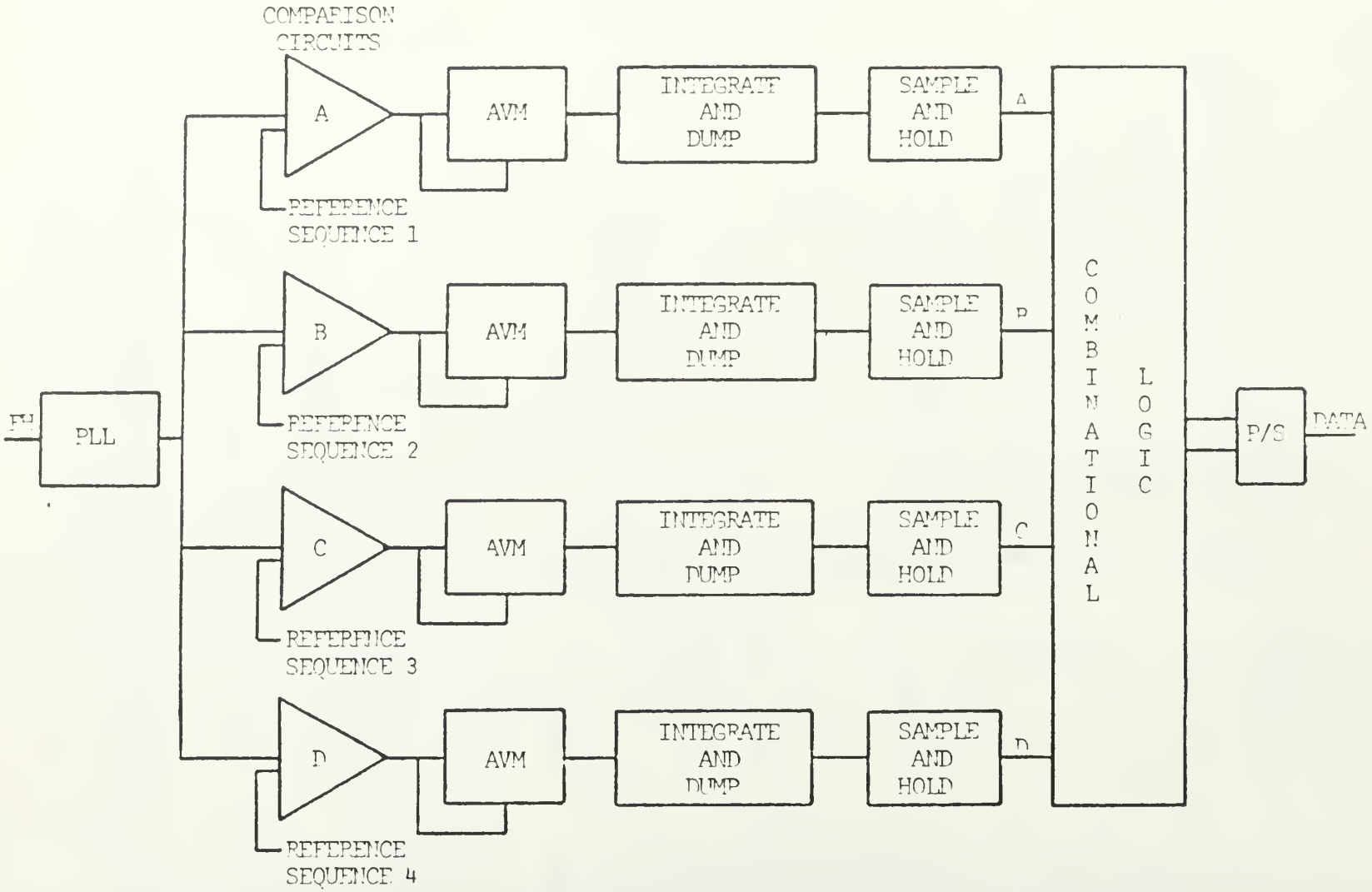

Figure 3.6 Receiver

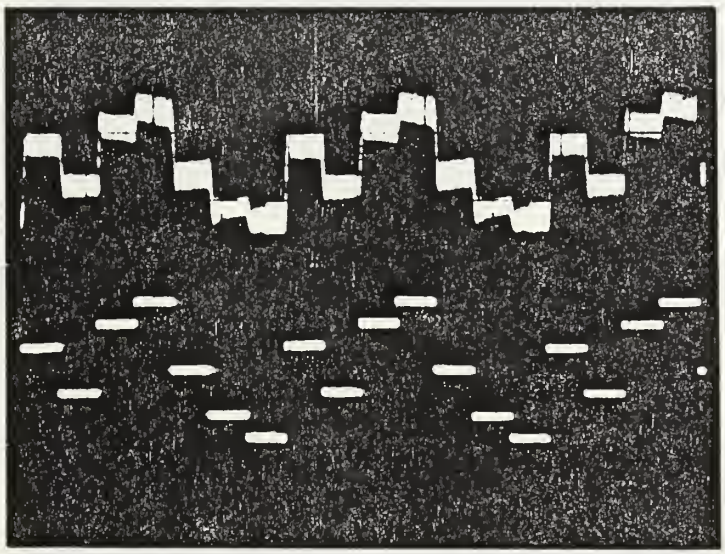

Figure 3.7
Top: PLL Cutput
Bottom: Transmitted VH Sequence

The comparison circuits generate the difference of the received and reference VH sequences with an op-amp circuit. The reference VH sequences are identical to the four VH sequences generated in the transmitter and would, in actuality, be stored in the receiver. The delay between the transmitter VH sequences and the PLL output, over the symbol interval, is observed to be negligible and, therefore, the transmitter sequences are used also as the receiver reference sequences. Figure 3.8 shows the difference voltages produced by comparing both like and unlike received and reference sequences. Both traces in Figure 3.8 are shown for one repeating transmitted symbol (two data bits). Zero and non-zero voltages are generated by comparing like and unlike sequences, respectively. Subsequently, for any symbol interval, only one of the four difference voltages is zero depending on the data word transmitted.

Each difference voltage is then squared using an analog voltage multiplier. The difference voltages in Figure 3.8 are shown squared in Figure 3.9. Squaring converts the bipolar difference voltage to a unipolar voltage. Additionally, squaring suppresses small voltages (low-level noise effects) and emphasizes large voltages resulting from the comparison of unlike sequences.

The squared difference voltages, which are now unipolar, are then integrated and sampled. Integration, performed over a symbol interval and then dumped, is accomplished by an op-amp integration circuit. The integration of the voltages shown in Figure 3.9 is presented in Figure 3.10. Just prior to the integration dump, the voltages are sampled and held for a symbol interval by a sample and hold circuit.

Depending on the data word (or symbol) transmitted, three of the four sample and hold output voltages are positive while the fourth is zero. A zero voltage, produced by

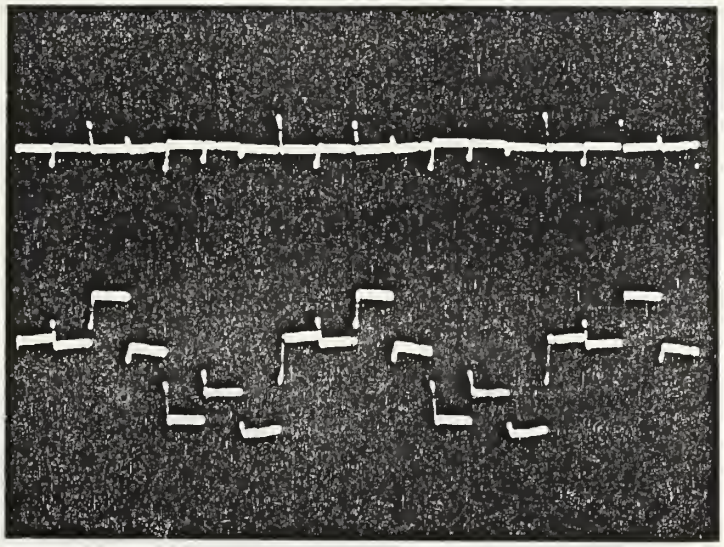

Figure 3.8
Top: Difference Voltage for Like Sequence
Bottom: Difference Voltage for Unlike Sequence

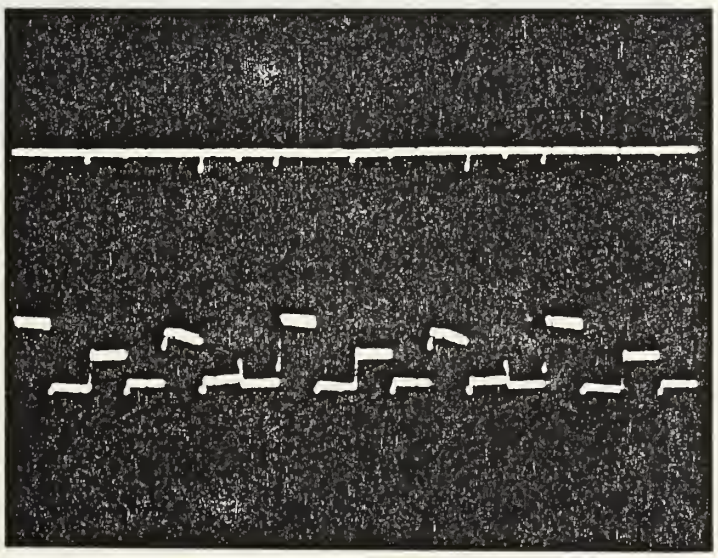

Figure 3.9 Squared Difference Voltages from Fig.3.8

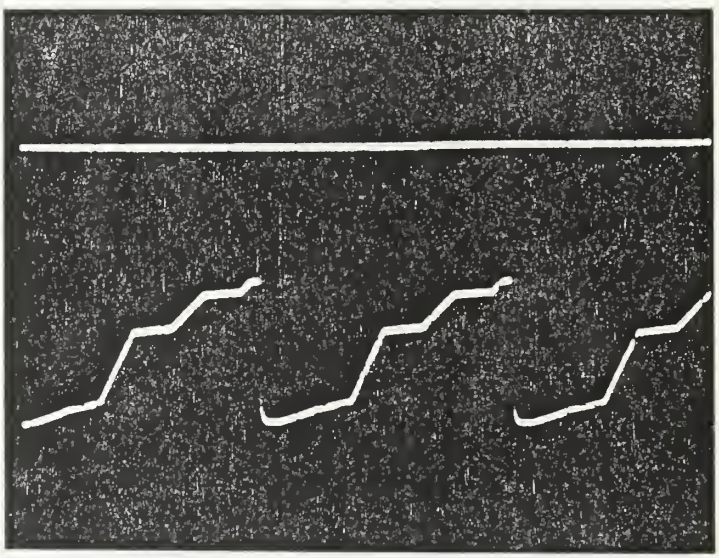

Figure 3.10 Integration of Squared Voltages from Fig.3.9

comparing like received and reference VH sequences, identifies the transmitted data word--the data word is that which corresponds to the reference VH sequence used in that branch of the receiver which generates a zero voltage.

The correct data word is generated by applying the output voltages of the sample and hold circuits to a five gate combinational logic circuit. The integration gains are adjusted and five volt zener diodes are used to make these output voltages compatible with digital circuitry, specifically transitor-transitor logic (TTL). A positive voltage at any sample and hold output is generated as a TTL logical "1" and a zero voltage is, likewise, generated as a TTL logical "0". The combinational logic uses these voltages to produce the appropriate data word (a two bit parallel output).

The combinational logic circuit consists of five TTL gates (see Figure C.6, Appendix C). For a zero voltage produced by a particular sample and hold circuit, the logic circuit generates the corresponding two bit data word. As an example, if sample and hold output A (see Figure 3.6) is low (logical "0") and outputs B, C, and D are high (logical "1"), then the logic circuit generates the correct data word: 00. If output B is low and outputs A, C, and D are high, then the data word 01 is generated and so on for the two other data words. The logic equations associated with the logic circuit are presented below.

$$(ABC) + (ACD) = \text{least significant bit}$$

$$\overline{(BCD) + (ACD)} = \text{most significant bit}$$

Finally, a parallel-to-serial converter is used to present the data bits serially. A detailed circuit schematic of the receiver is presented in Appendix C.

4. Error Detection Circuit

The error detection circuit provides bit error information to determine probability of error. The transmitted data is delayed and applied to a two input Exclusive-Or gate along with the received data. A logical "0" is generated if the transmitted and received bits are the same and a logical "1" if they are different. This logical "1" represents a bit error and is counted. Data bits are also counted. The bit error count to data bit count ratio is used as the probability of error. The circuit schematic for this circuit is shown in Appendix D.

IV. PERFORMANCE

A. EXPERIMENTAL PROCEDURE

1. System Parameters

To test the experimental system, adjustments or settings are made in the transmitter and receiver. After applying power, resetting all FSR's, and enabling the Data FSR, the master clock (MC) is set to a frequency of 6.8 kHz. Therefore, the data rate (or the frequency of MC/7) is approximately 971 bits per second.

The transmitter VCO is adjusted for a center frequency of 88 kHz. 5.47 kHz separates the individual hopping frequencies by the adjustment of the gain of the VH sequence input to the VCO. Consequently, the FH signal is composed of seven evenly spaced hopping frequencies ranging from 71.4 kHz to 104.2 kHz. The total bandwidth (BW) of the FH signal centered at 88 kHz is calculated below.

$$BW = 104.2 \text{ kHz} - 71.4 \text{ kHz} + 2(1/T)$$

$$= 32.8 \text{ kHz} + 2(1/294 \text{ microseconds})$$

$$= 39.6 \text{ kHz}$$

where T = the dwell time for one hop. Since the spectral occupancy of the transmitted signal is 68.2 kHz to 107.8 kHz, the upper and lower cutoff frequencies of the receiver bandpass filter (BPF) can be adjusted accordingly. Due to the non-constant frequency response of the Krohn-Hite BPF over the pass band, constant amplitudes for all seven frequencies were obtained by widening the pass band--66 kHz

= the lower cutoff frequency, 140 kHz = upper cutoff frequency.

In order for the receiver combinational logic to generate the correct two bit data word, a TTL logical "1" or "0" produced by the sample and hold circuits must be within the correct TTL voltage limits (0 to 0.8V for a logical "0", 2.4 to 5.0V for a logical "1"). The integrator 5V zener diodes limit the voltages to a maximum of +5V. In the absence of channel noise, the sample and hold voltages are minimum. This is due to the squaring of the difference voltages by the AVM. Channel noise, contaminating the comparison circuit output, is also squared (rectified) by the AVM and therefore, only increases the amplitude of the squared difference voltage. When a larger amount of channel noise is present, both sampled voltages, generated by comparing like as well as unlike sequences, increase. With no channel noise present, each of the four integrator gains are adjusted so that sampled voltages from like sequence comparisons are set to the lower limit of the TTL logical "0" and those from unlike sequence comparisons are set to the lower limit of the TTL logical "1". Because the integration time varies with data rate, a change in data rate requires a change in integrator gain. This gain adjustment allows voltages, from unlike sequence comparisons, to vary from 2.4 to 5.0V. Voltages from like sequence comparisons, however, may vary from 0V to voltages greater than 0.8V. As an input to the receiver combinational logic, this voltage excursion above 0.8V (due to noise), for like sequence comparisons, unavoidably degrades receiver performance.

After some testing of the system with the integrator gain adjusted as discussed in the preceeding paragraph, a modification was made to the receiver. Noting that an error could occur if a voltage from a like sequence comparison were to increase from 0V to a voltage greater than 0.8V, the

integrate and dump circuits are reconfigured to lower the value of the logical "0" lower limit. A 2.3V voltage source and a 3 kilohm resistor are connected to the inverting input of the op-amp integrator (see Figure C.4, Appendix C) to bias the output low by approximately 1.7V. As shown in Figure 4.1, this allows a voltage from a like sequence comparison to increase from -1.7V to 0.8V before causing an error. (As in the original configuration, the integrator gain is adjusted, in the absence of noise, so that the voltages generated from unlike and like sequence comparisons are set to their lower limits--2.4V and -1.7V, respectively.) This modification effectively expands the "decision region" for the logical "0" thus allowing more "room" for noise generated voltage excursions before 0.8V is exceeded. Diodes connected to the output of the integrator insure that 0V is the lowest voltage applied to the TTL combinational logic.

The experimental system, using the expanded decision region, is superior to the original system configuration. A 1.5 dB signal to noise ratio (SNR) improvement is obtained at a bit probability of error of 0.001.

2. Measured Performance

In this research, the probability of error is determined for different values of SNR. The SNR is measured using a true RMS voltmeter. The RMS voltage (s) of the signal and the RMS voltage (k) of the signal plus noise are measured. For all measurements, s = 0.2V. SNR is calculated as follows:

$$\text{Signal power} = S = s^2$$

$$\text{Noise power} = N = k^2 - s^2$$

$$\text{SNR (dB)} = 10 \log (S/N)$$

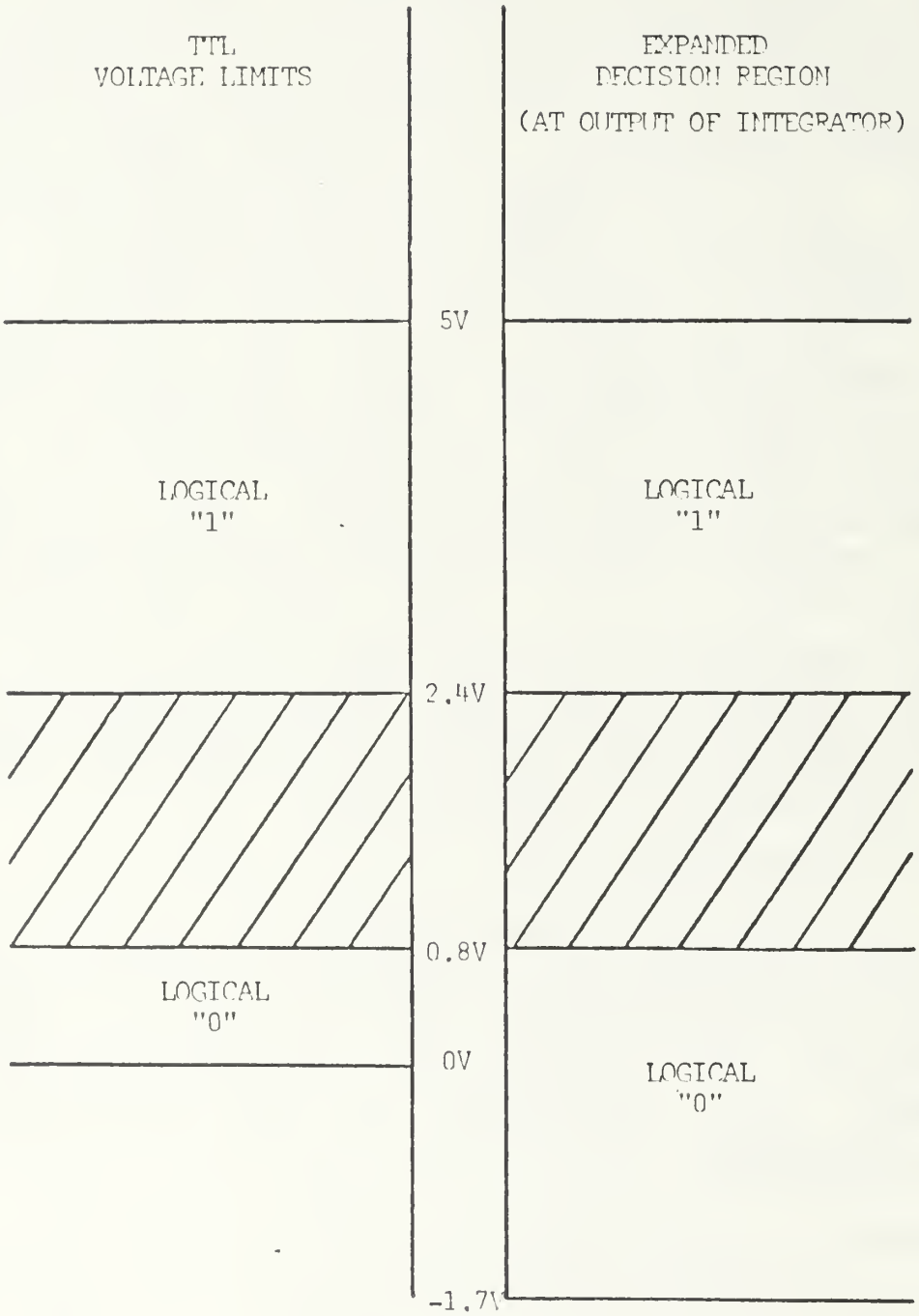

Figure 4.1 Decision Space

For a measured SNR,

probability of error = bit errors / bits transmitted

where the number of bits in error and the number of bits transmitted are obtained from the error detection circuit. For each determination of probability of error for a given SNR, the number of bit errors is counted for approximately one million bits transmitted.

B. RESULTS

Figure 4.2 shows the five experimental probability of errors curves. All five curves are obtained at a system data rate of 971 bits per second using the expanded decision region as discussed in the previous section. Each curve is plotted using at least twelve data points.

In addition to data for probability of error vs. SNR using Gaussian noise, system performance in the presence of tone jamming is also measured. Tones, selected from the seven frequencies used in the transmitted signal, are produced by separate signal generators and are added to the signal in the system channel. Therefore, signal to jamming ratio (SJR) is measured in the same manner as SNR.

The curves in Figure 4.1 indicate better system performance in the presence of high frequency single-tone jamming. The LM565 PLL characteristically produces a low voltage for a high frequency input and a high voltage for a low frequency input. High frequency jamming generates a low voltage component in the PLL output that, in turn, has a smaller effect on the generated difference voltages. Two-tone jamming (power in tones equally split) further degrades the performance of the receiver.

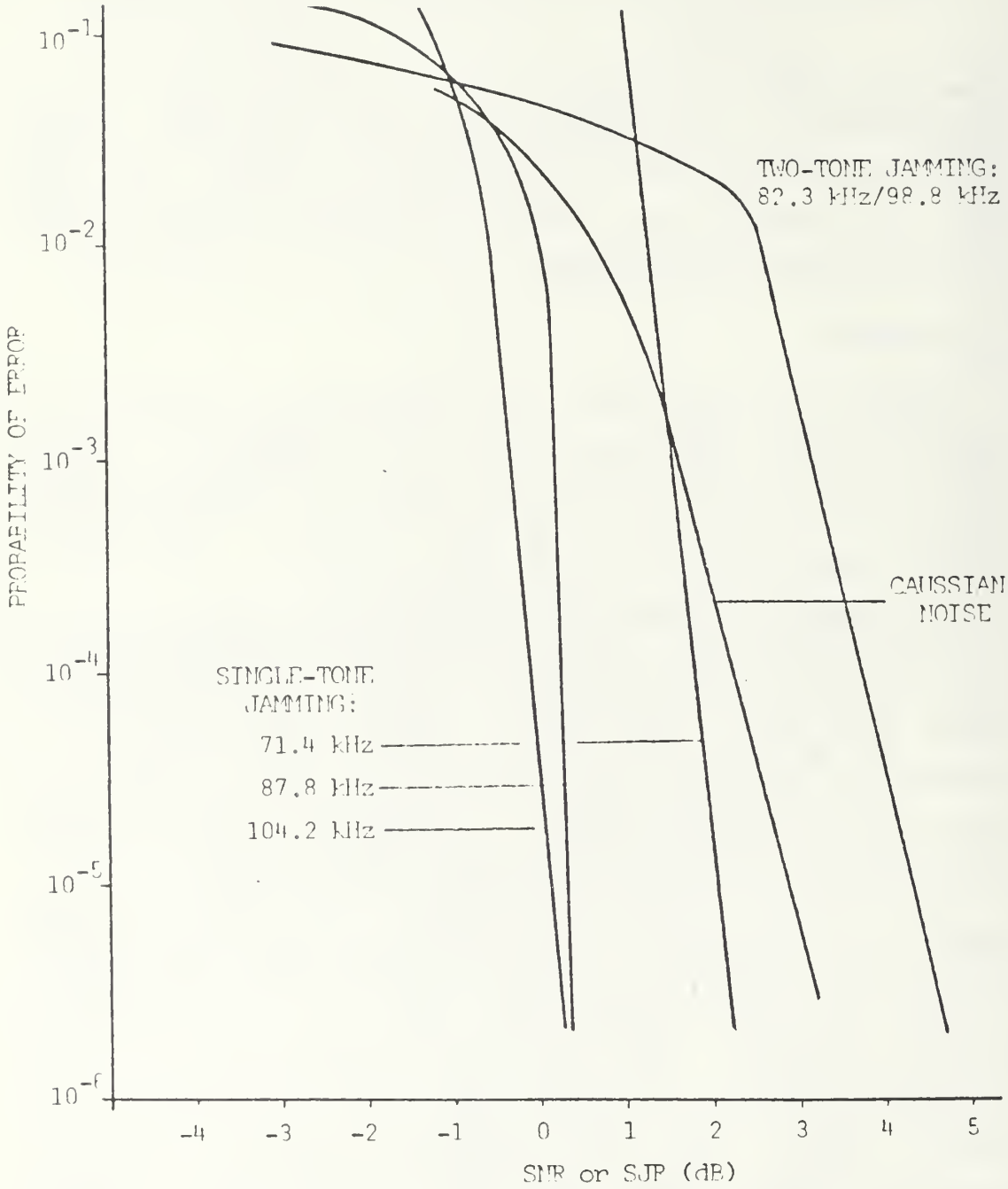

Figure 4.2 Experimental Results

V. CONCLUSIONS AND RECOMMENDATIONS

The major benefit from using a multiple hop sequence FH scheme is the flexibility in symbol representation. The number of data bits per symbol (m) represented by a particular sequence may be varied. Perhaps more significant is the ability to vary the number of hops per sequence (H) independent of m.

The receiver, performing well, has two design advantages. First, the receiver design is relatively simple. Increasing the number of sequences and addressing the problem of synchronization will increase complexity, but the basic receiver design is simple. Second, two major components of the receiver help to minimize noise. The analog voltage multiplier reduces noise present in the difference voltages and the integrator reduces noise by providing processing gain (the integrate and dump circuit is a matched filter realization).

Further testing of this system is recommended. Receiver performance in the presence of different tone jamming schemes could be evaluated as well as receiver synchronization and it's effect on performance.

APPENDIX A
TRANSMITTER CIRCUIT SCHEMATIC

Appendices A, B, C, and D contain the schematic diagrams for the experimental system. In the diagrams, all resistor values are in kilohms and capacitor values are in microfarads. Specifications for the digital and analog integrated circuits can be found in References 3, 4, and 5.

Figures A.1 and A.2 show the clock circuits and reset switch. The three generated clock signals, in Figure A.1, are used in both the transmitter and receiver. The master clock (MC), produced by a Wavetek 142 signal generator, is set at 6.8 kHz. The frequency of the MC is divided in half by a JK flip-flop to obtain MC/2. Dividing the frequencies of MC and MC/2 by seven, MC/7 and MC/14, respectively, are produced. A 4 bit parallel load counter accomplishes the division by seven. The counter is loaded by the carry out and RESET so that every seventh clock pulse will activate the carry out signal. The reset switch allows MC/2 to reset the divide-by-seven circuits, the FSR's of the HSG, and the Data FSR within the positive cycle of the clock but away from the triggering edge. This insures that all are reset on the same clock cycle. The reset switch uses a double-pole double-throw switch, an RS flip-flop, and MC/2 to generate the RESET signal (Figure A.2).

A hop sequence generator (HSG) is shown in Figure A.3. There are four HSG's in the transmitter--one for each symbol. Which of the four different VH sequences are produced by the DAC is determined by the word loaded into the FSR upon reset (see table below FSR in Figure A.3). Figure A.3 also shows the feedback connections to the Exclusive-Or gate for each symbol.

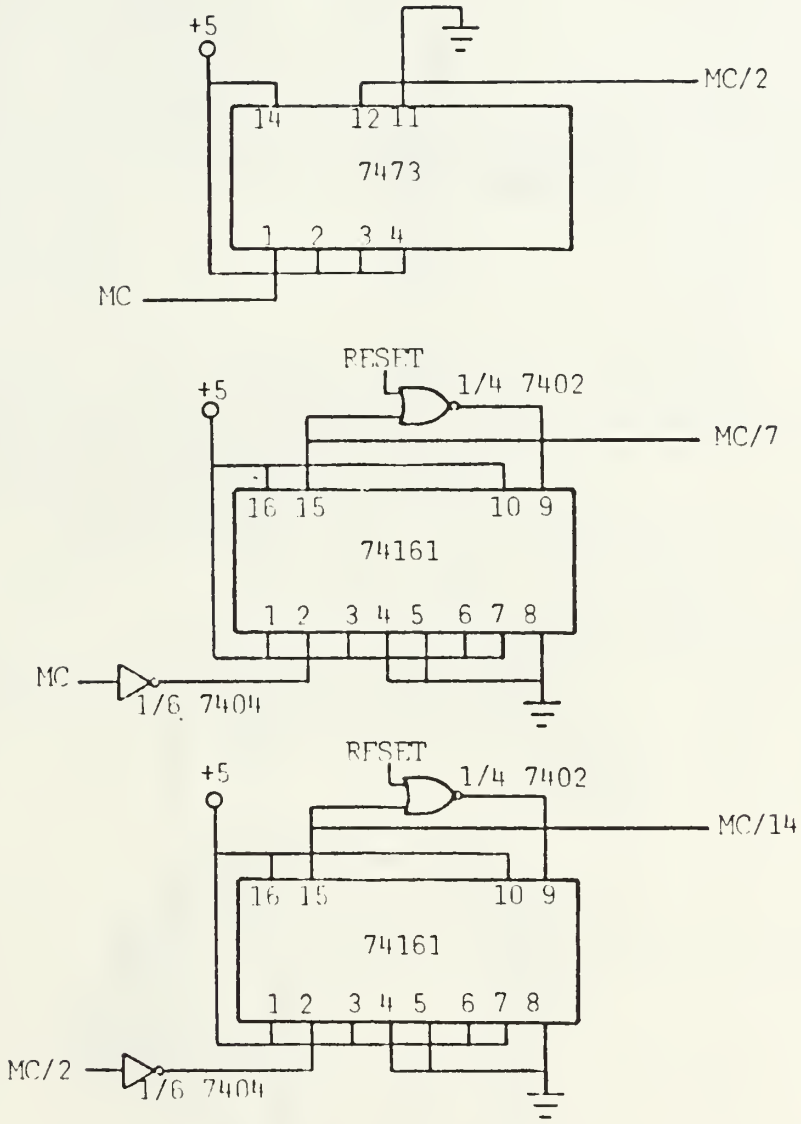

Figure A.1 Clock Circuits

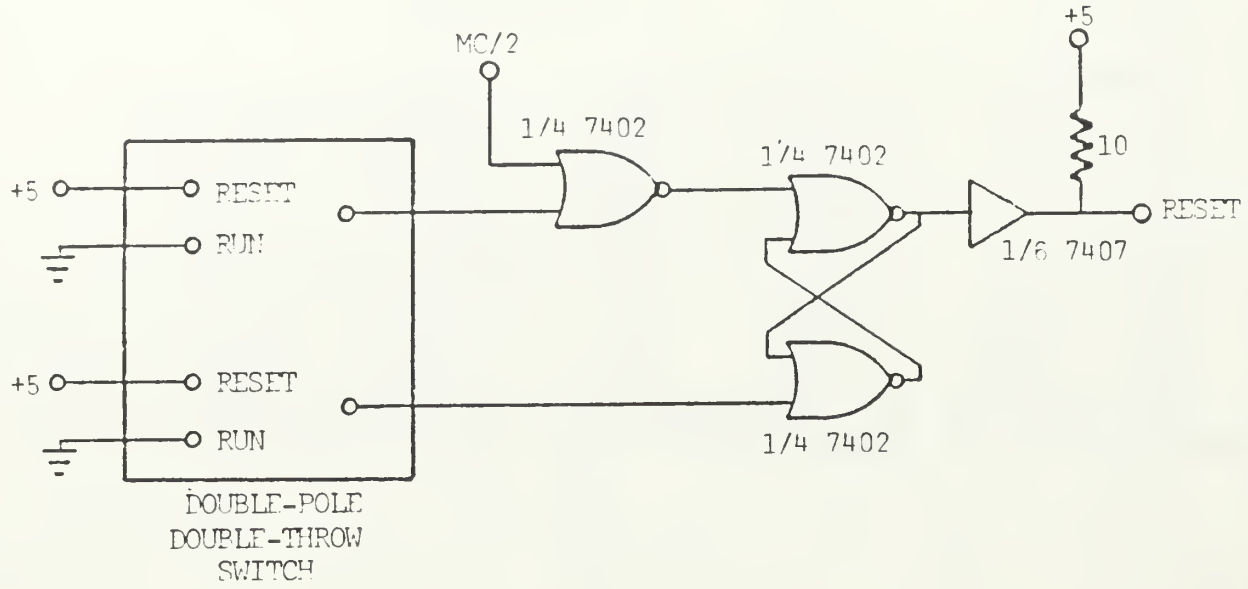

Figure A.2 Reset Switch

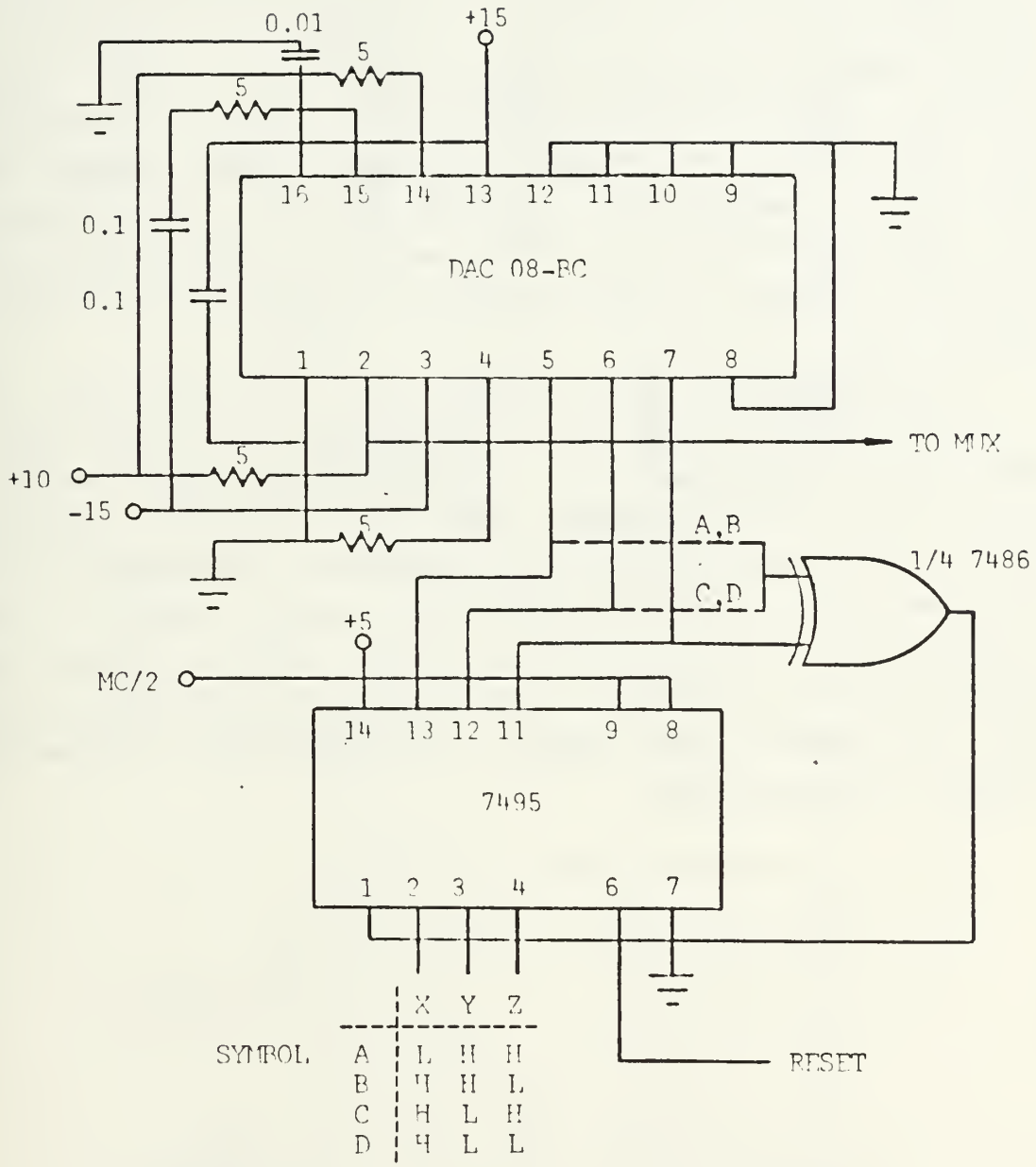

Figure A.3 Hop Sequence Generator

Figure A.4 shows the Data FSR and buffer circuit. Using a [7,1] feedback tap to produce a 127 bit m-sequence, the two bits, for the data word, are taken from the two adjacent registers of the FSR--5 and 6. By using two D-type flip-flops (buffer circuit) and appropriate clock signal (inverted MC/14), the two data bits, d1 and d2, are obtained from the 127 bit m- sequence without overlap between two data words. Neither are any bits skipped. Additionally, the eighth register of the FSR (pin 13) is used in the error detection circuit as the serial presentation of the transmitted data.

Comparators are used (Figure A.5) to change the TTL levels of the data bits to those compatible with CMOS logic. Depending on the data bits, the multiplexer (MUX) selects one of the four VH sequences (applied to the four channels of the MUX from the HSG's) and passes the sequence to two cascaded op amp circuits (Figure A.6) then, the VCO. The variable gain of the first op amp is used to adjust the frequency hop interval of the FH signal generated by the VCO. The second op amp inverts the sequence for the desired sequence configuration.

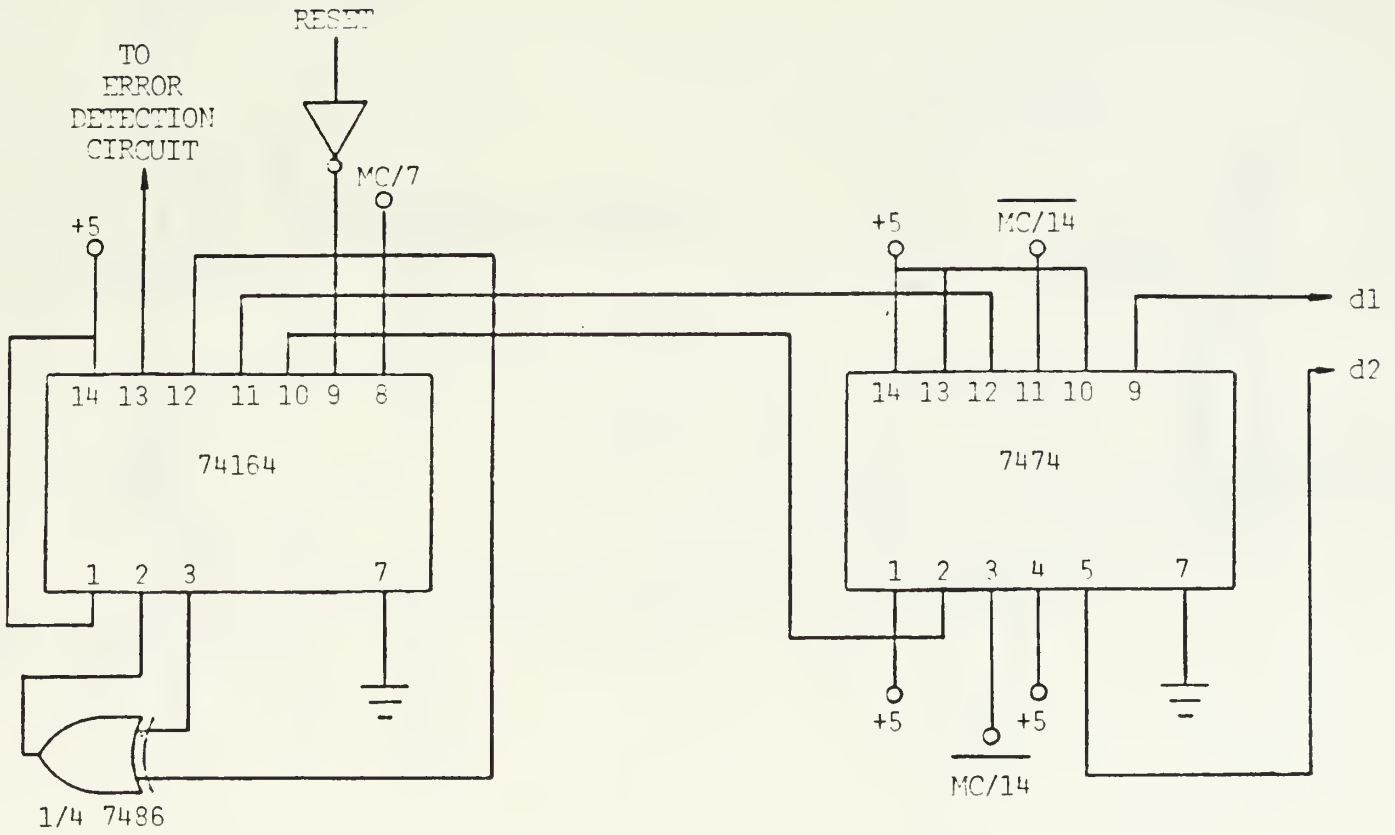

Figure A.4 Data FSR and Buffer Circuit

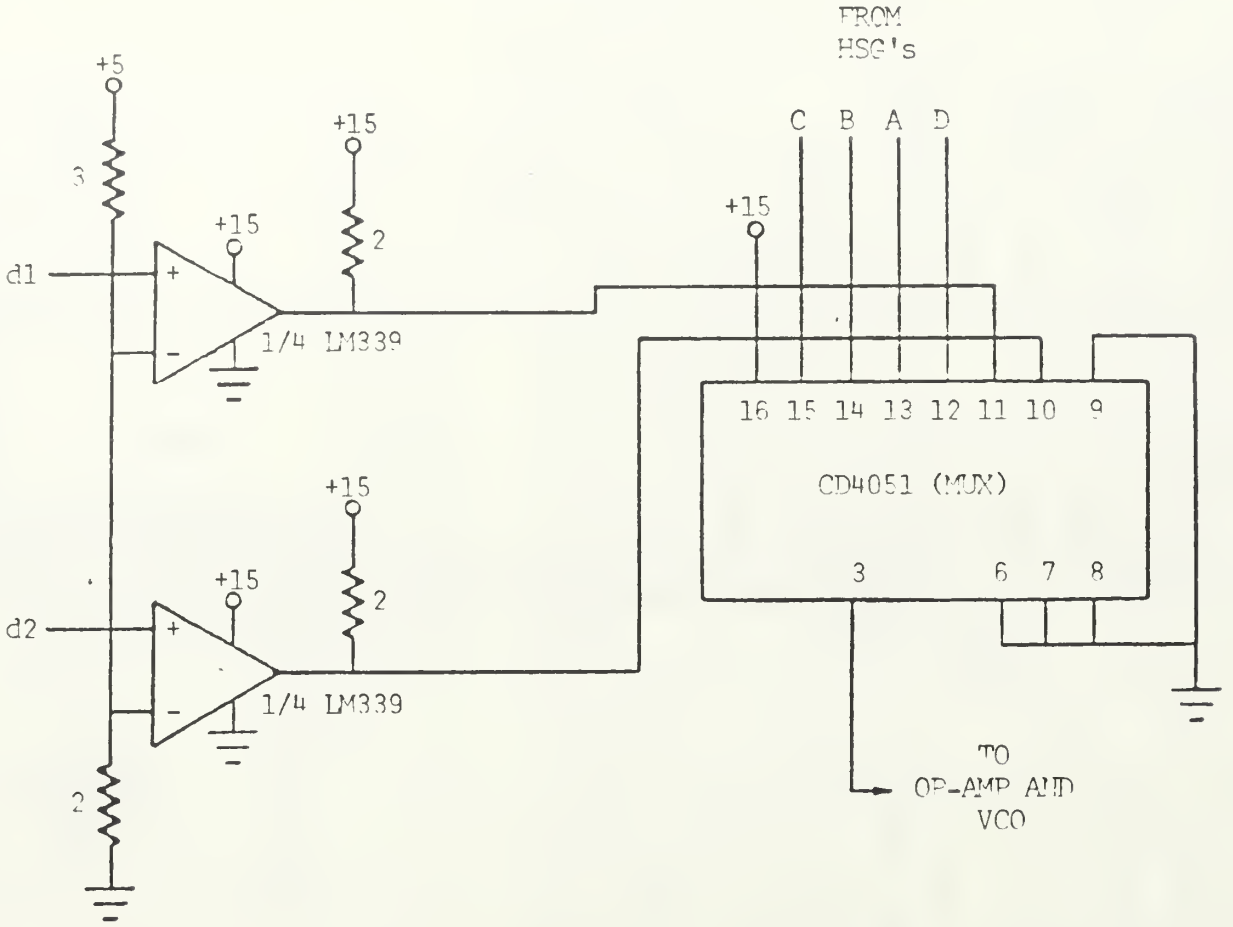

Figure A.5 Sequence Selection Circuit

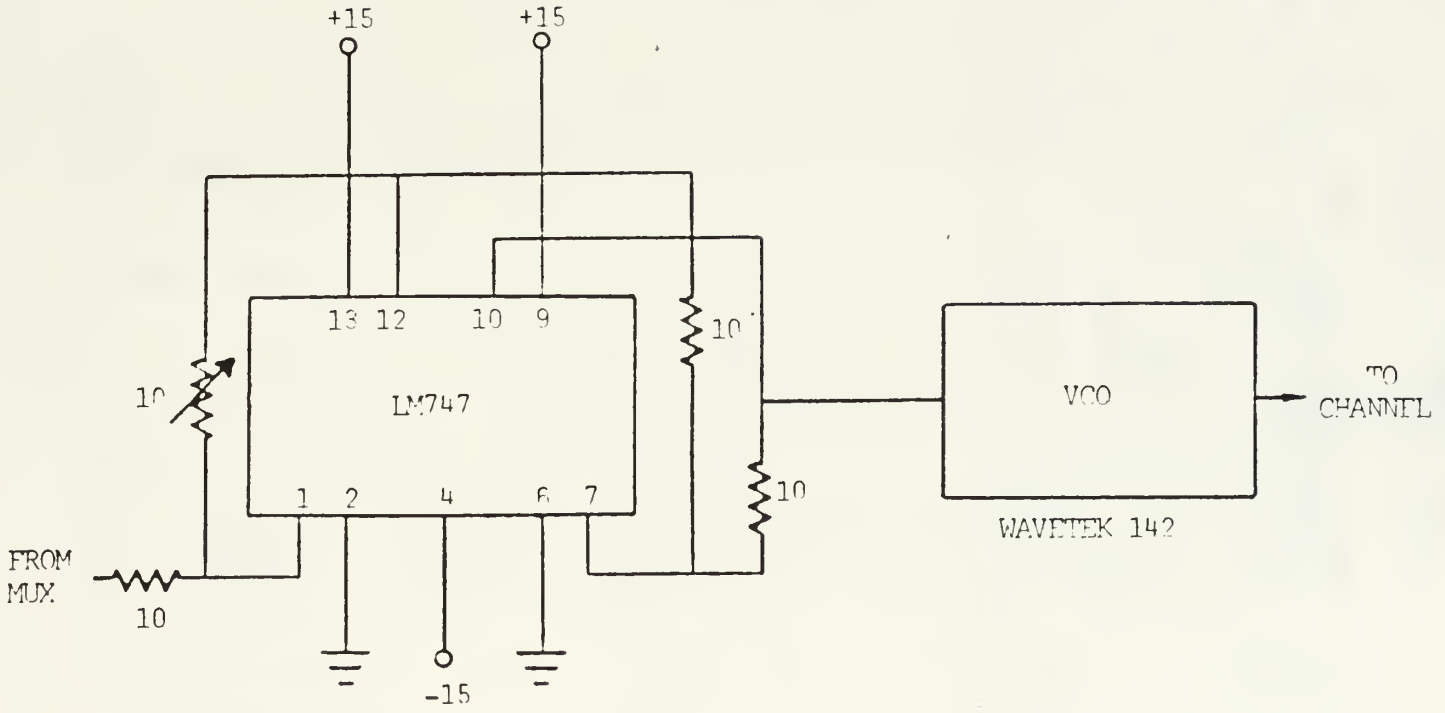

Figure A.6 Modulator

APPENDIX B
CHANNEL CIRCUIT SCHEMATIC

Figure B.1 shows the circuit used to simulate the channel in the experimental system. The transmitted FH signal is added to wideband Gaussian noise by an op amp adder (gain = -1). The combined signal and noise is then applied to the front end of the receiver--a BPF configured to pass the FH signal with minimum distortion (see Chapter IV for details concerning spectral occupancy of the FH signal). The filtered signal and noise is then delivered to the PIL.

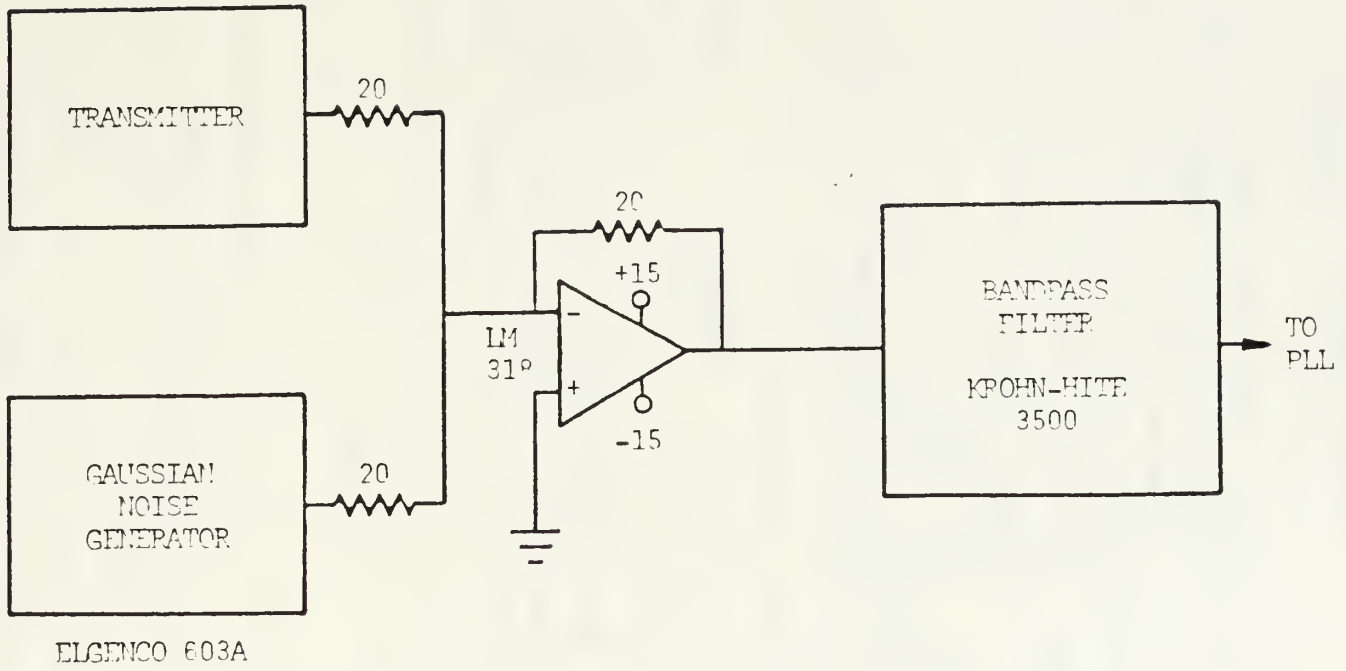

Figure B.1 Channel

APPENDIX C
RECEIVER CIRCUIT SCHEMATIC

The phase locked loop (PLL) used in the receiver is a National Semiconductor LM565 PLI (Figure C.1). The PLL is configured for a free-running or center frequency of 88 kHz (the center frequency of the FH signal). Consequently, the hold-in range of the PLL is 17.2 to 154.8 kHz--sufficient to cover the bandwidth of the transmitted FH signal (see Chapter IV). The output of the PLL is filtered with an RC lowpass filter and a capacitor removes the D.C. bias.

Figure C.2 shows one of the four comparison circuits. Because the PLL characteristically generates an inverted VH signal than that delivered to the input of the transmitter VCO, the PLL output is simply added to each of the four transmitter HSG outputs to produce the difference voltage. An op amp adder and adjustable voltage divider networks are used to sum these two signals. A D.C. blocking capacitor, voltage follower, and RC lowpass filter are connected to the op amp output to reduce noise and minimize distortion.

Each of the four difference voltages are squared with an analog voltage multiplier (Figure C.3). The 20 kilohm potentiometer is adjusted for desired peak output signal level.

The output of the analog voltage multiplier is applied to an integrate and dump circuit (Figure C.4). An op-amp integrator with adjustable gain is used for integration. As discussed in Chapter IV, a 2.3V voltage source and a 3 kilohm resistor are connected to the inverting input of the op-amp integrator to bias the output low by approximately 1.7V. The integration is dumped by shorting the feedback capacitor at the end of the symbol interval. MC/2 and MC/14

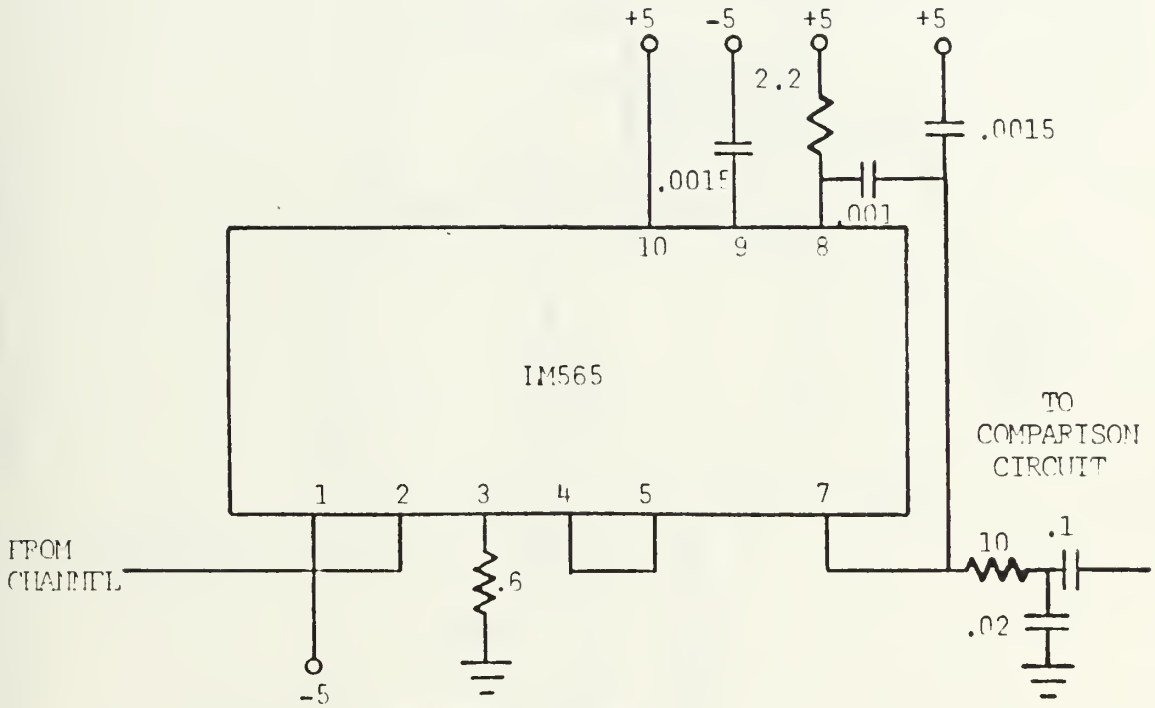

Figure C.1 Phase Locked Loop

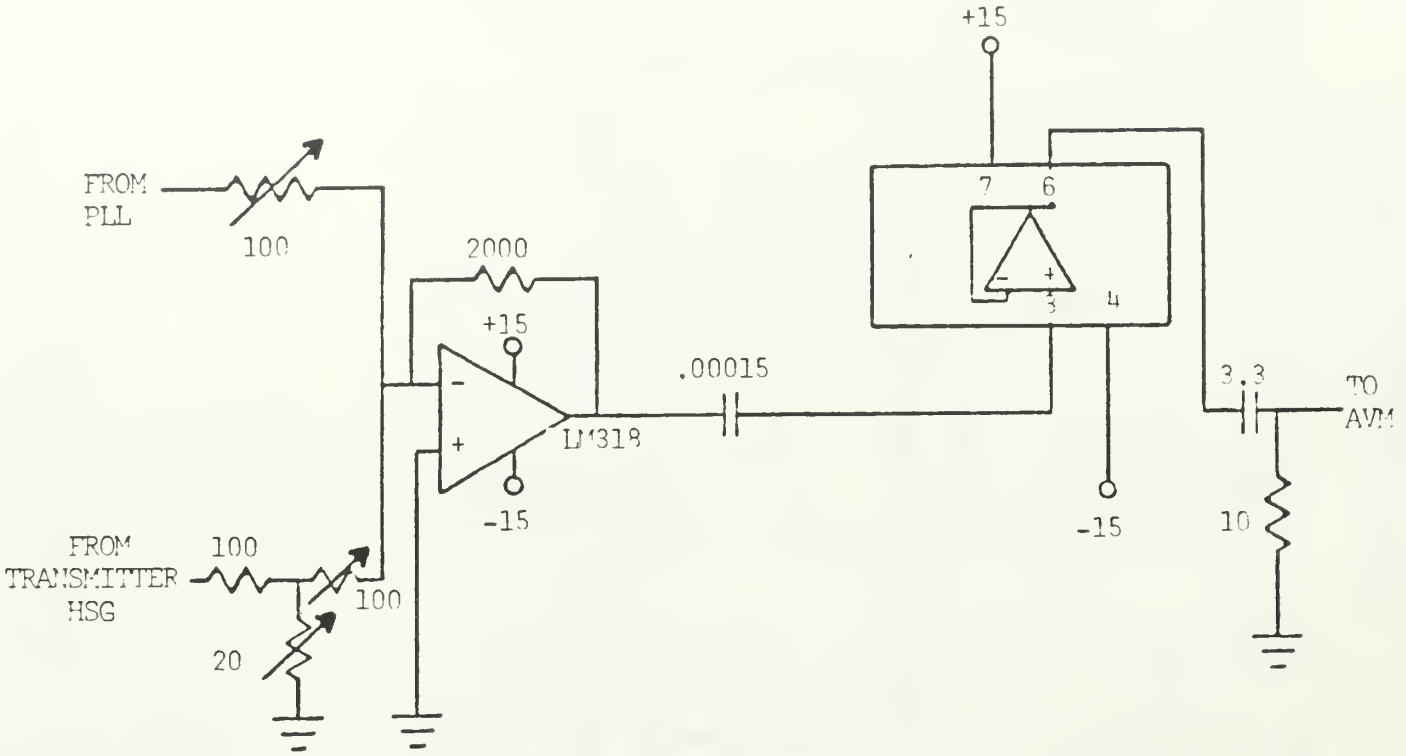

Figure C.2 Comparison Circuit

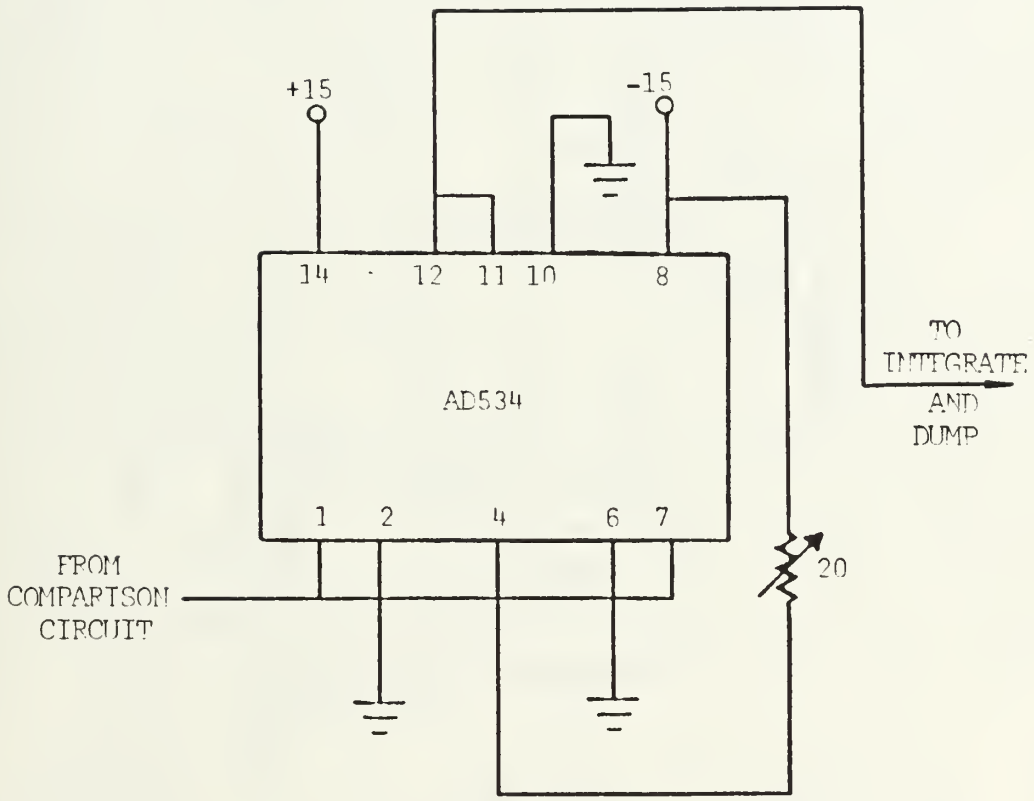

Figure C.3 Squaring Circuit

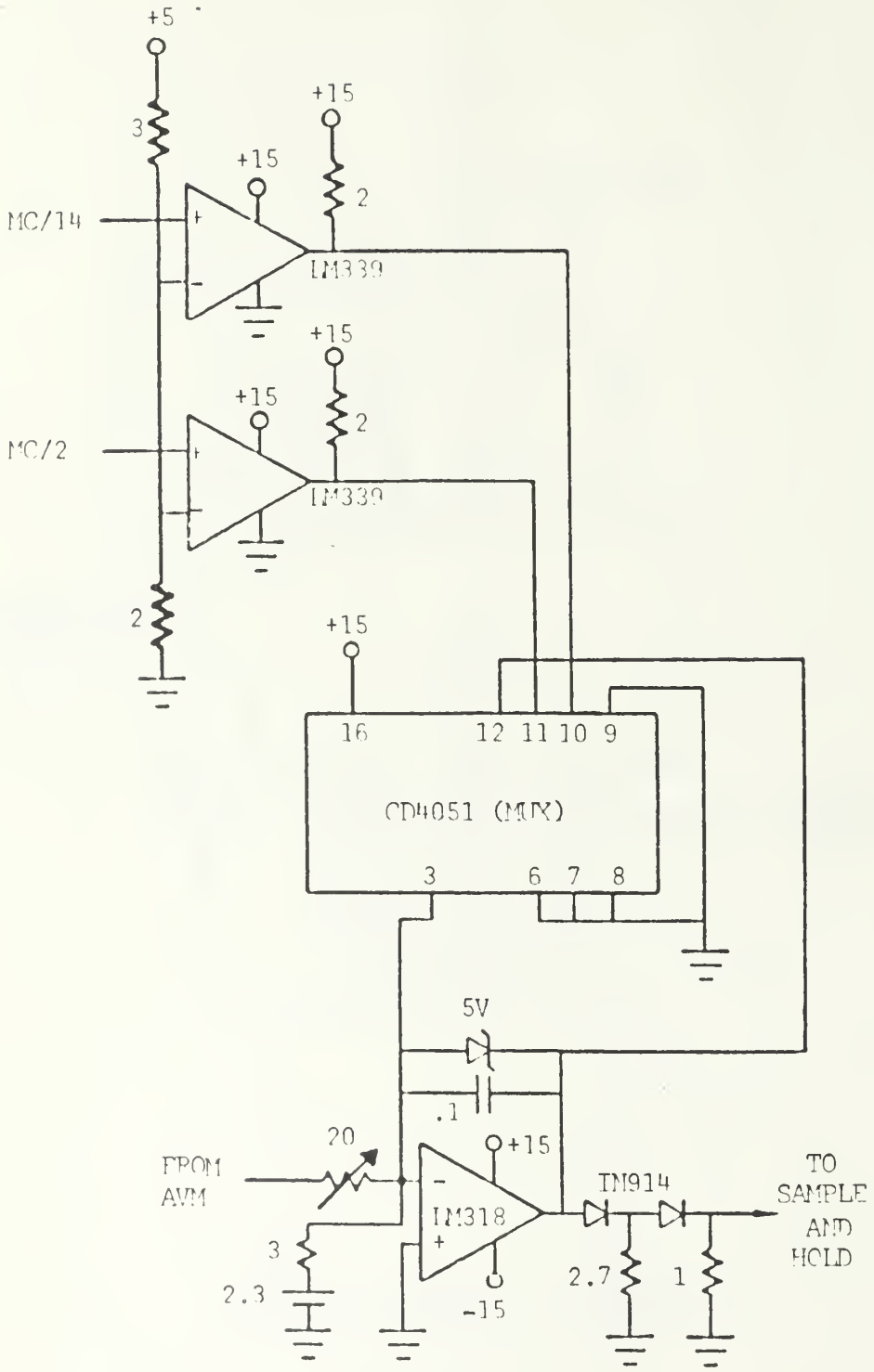

Figure C.4 Integrate and Dump Circuit

(made CMOS compatible by a comparator circuit) are both high at the end of the symbol interval and are used to activate the channel of the multiplexer that completes the short. A 5V zener diode limits the output voltage to a range of 0 to 5V. Two cascaded envelope detectors are used at the output to reduce noise and limit the output voltage to 0V (lower limit).

Figure C.5 shows a sample and hold circuit (National Semiconductor LF398) and the circuitry to generate the sample pulse. The sample pulse is produced by applying MC/14 and inverted MC/2 to an AND gate creating a pulse just prior to the time of the integration dump. The sampled voltage is held until the next sample pulse.

The outputs of the four sample and hold circuits, now TTL compatible by the use of the 5V zener diodes in the integrator circuits, are applied to the combinational logic circuit (Figure C.6). The labels for the sample and hold outputs (A, B, C, and D) indicate the reference VH sequence used in that branch of the receiver (in the comparison circuit). With the low sample and hold output indicating the received data word, the combinational logic generates the correct two-bit data word. For example, if A is low and B, C, and D are high, the received data word is 00 (symbol A).

Figure C.7 shows the parallel to serial converter. The circuit makes use of the inverted MC/14, sample pulse, and MC/7 to convert the parallel data bits, d1' and d2', to serial form.

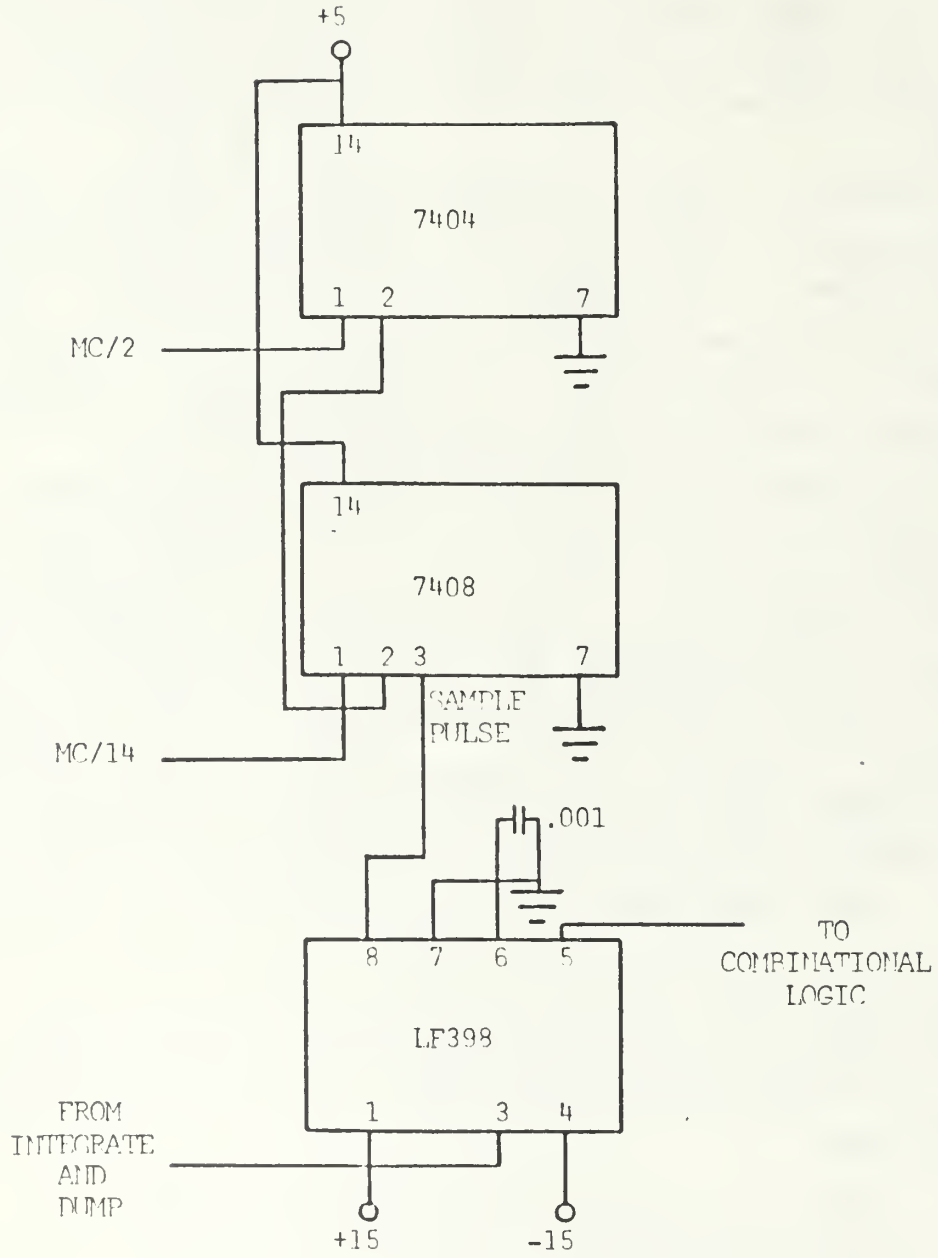

Figure C.5 Sample and Hold Circuit

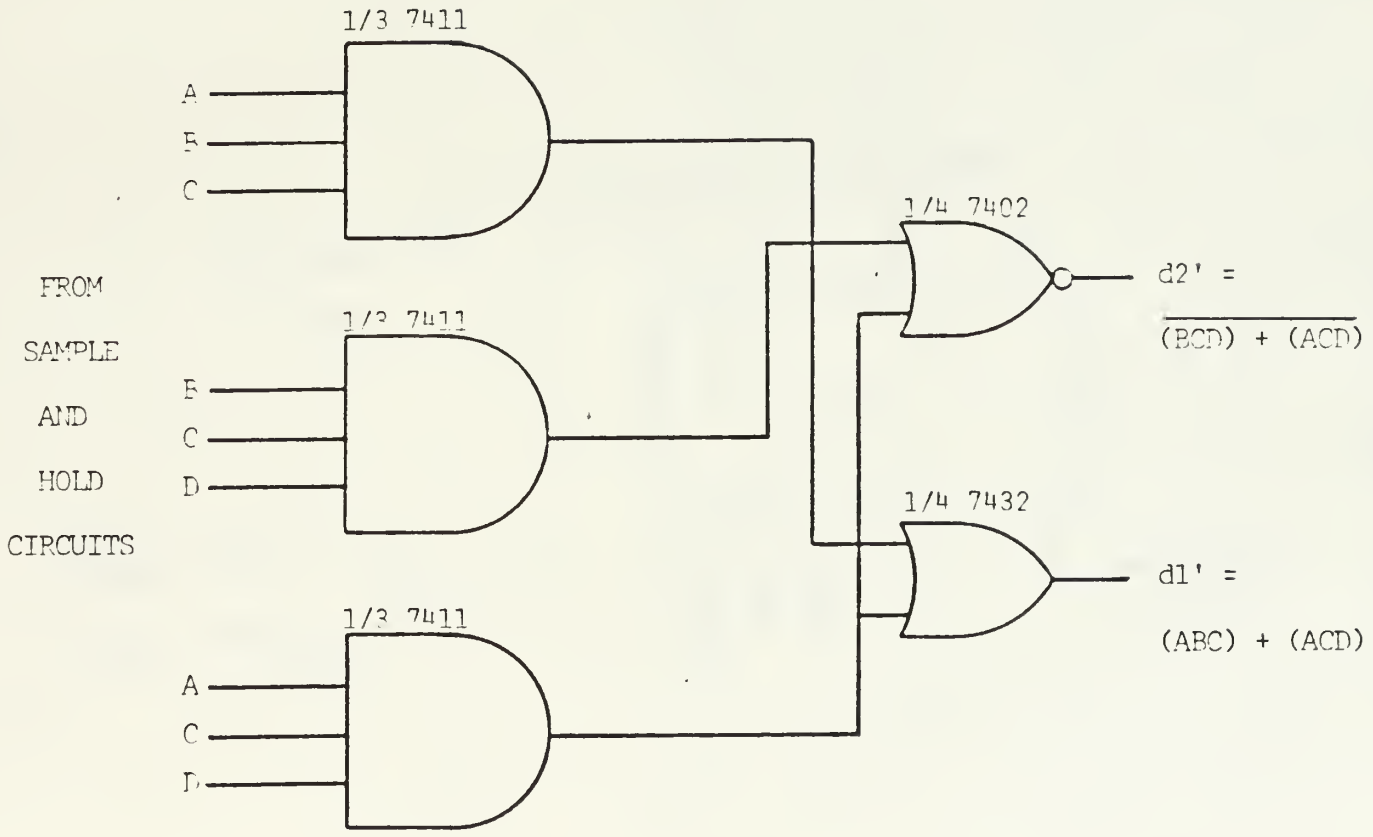

Figure C.6 Combinational Logic

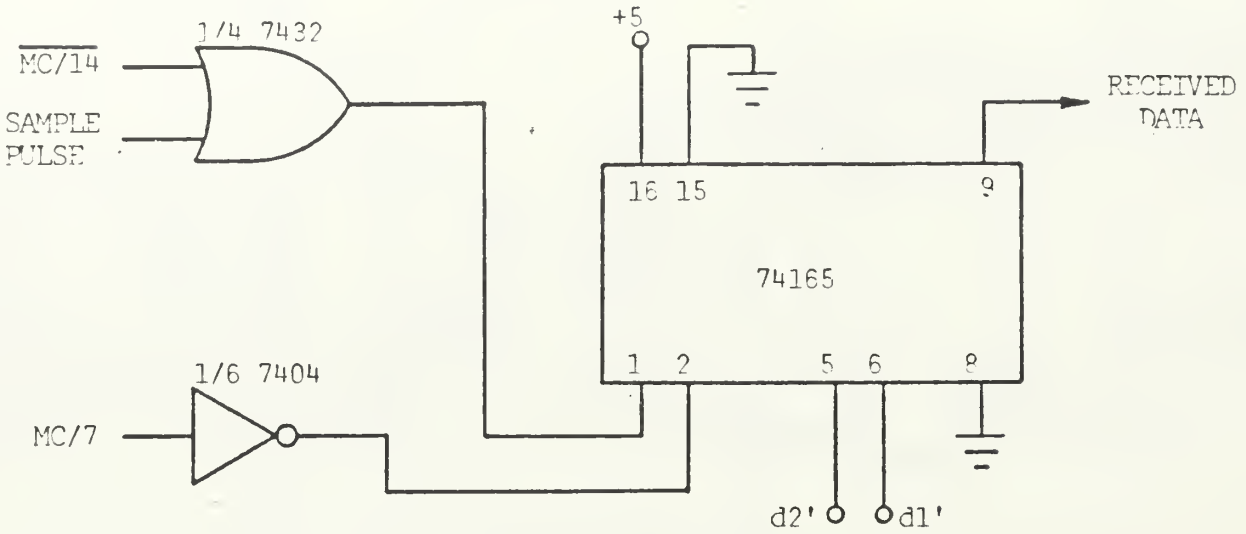

Figure C.7 Parallel to Serial Converter

APPENDIX D
ERROR DETECTION CIRCUIT SCHEMATIC

The error detection circuit is shown in Figure D.1. The transmitted data is obtained from the eighth register of the transmitter Data FSR and has an appropriate time delay so that a direct comparison with the received data can be made. The transmitted and received data are applied to an Exclusive-Or gate. If the two compared bits are different, a logical "1" is generated--a "0" if they are alike. Every logical "1" indicates a bit error and is counted. To insure the bit comparison occurs when the transmitted and received data bits overlap in time, the Exclusive-Or gate output is strobed in the middle of the time overlap by the use of a monostable multivibrator and an AND gate. The number of bits transmitted is determined by counting the positive pulses of MC/7 (or, equivalently, the data rate clock).

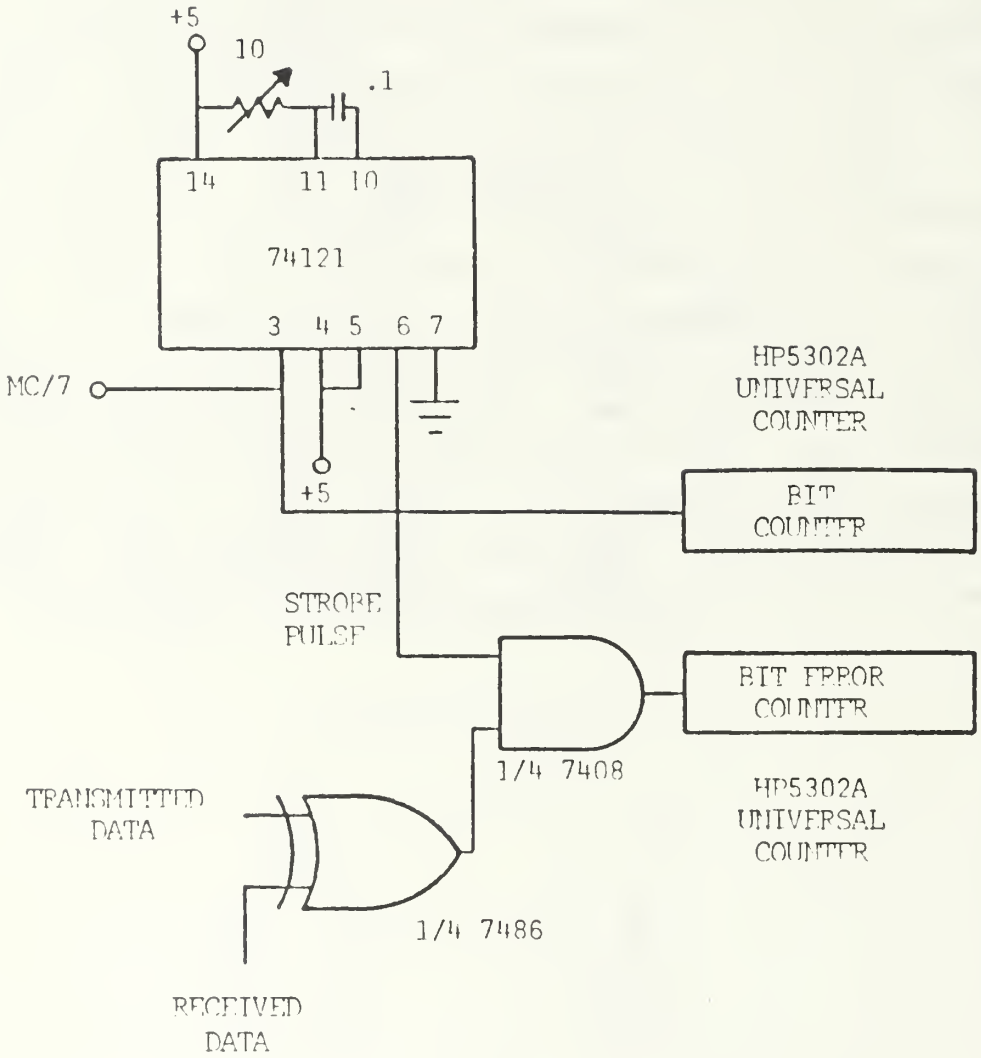

Figure D.1 Error Detection Circuit

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